SEU Mitigation
Truth Table

TR0	TR1	TR2	V
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Triple Redundancy with Voting

FIG. 1   FIG. 2
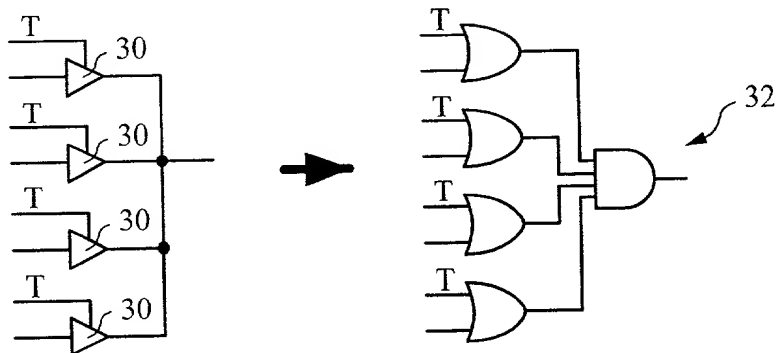
Virtex BUFT Structure

FIG. 3
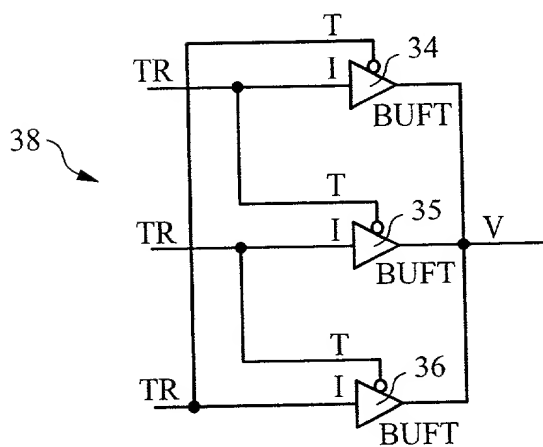
Voting circuit with BUFTs

FIG. 4

TRV Truth Table

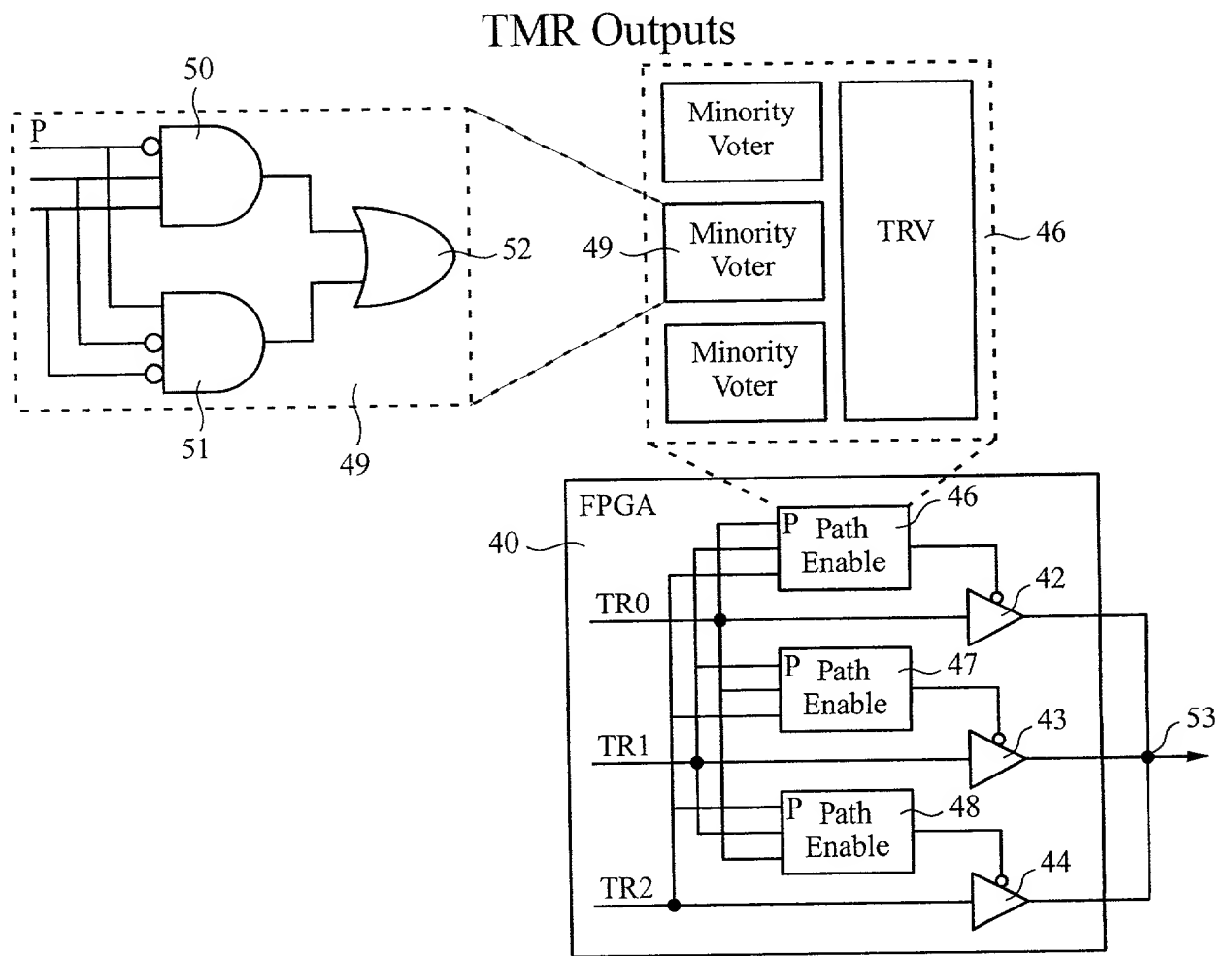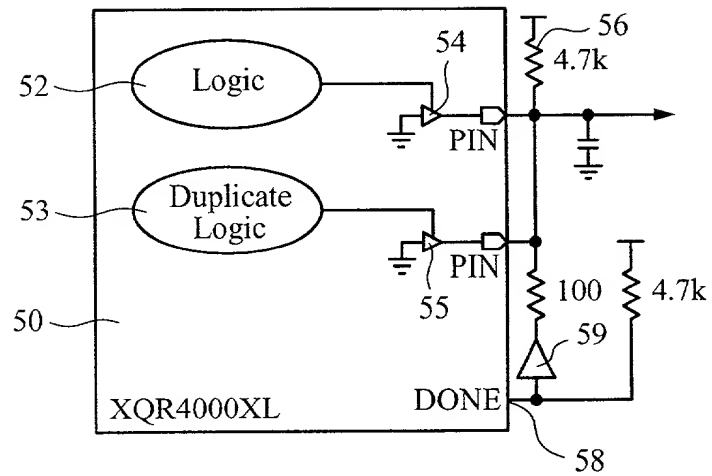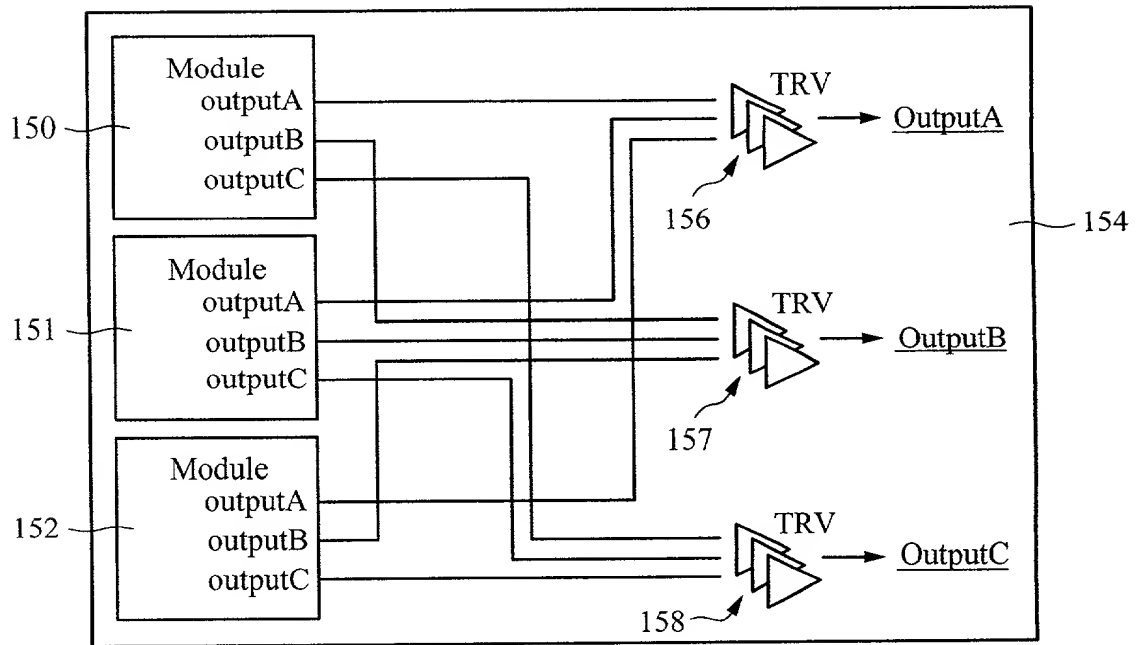| TR0	TR1	TR2	V
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

FIG. 5

TMR Outputs

FIG. 6

Wire-ANDing Critical Outputs

FIG. 7

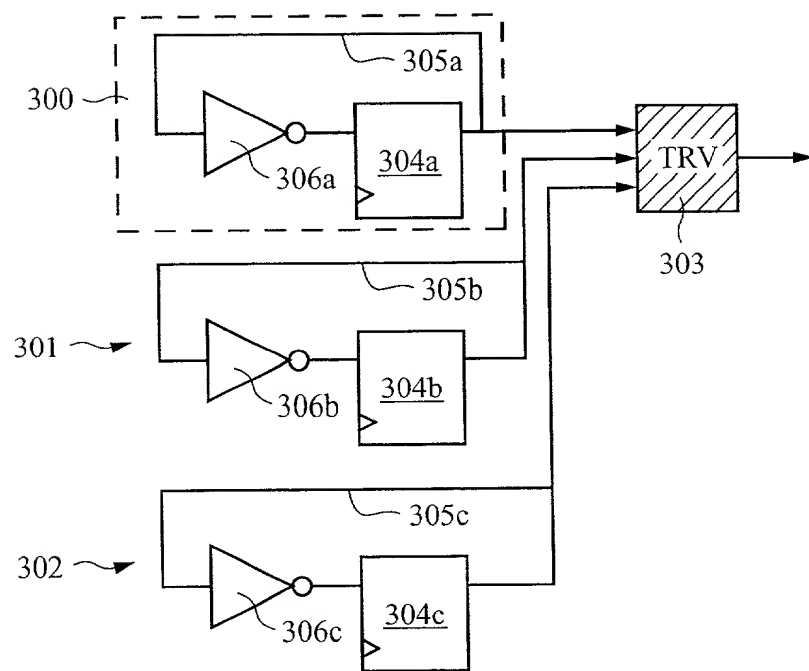Module redundancy and mitigation
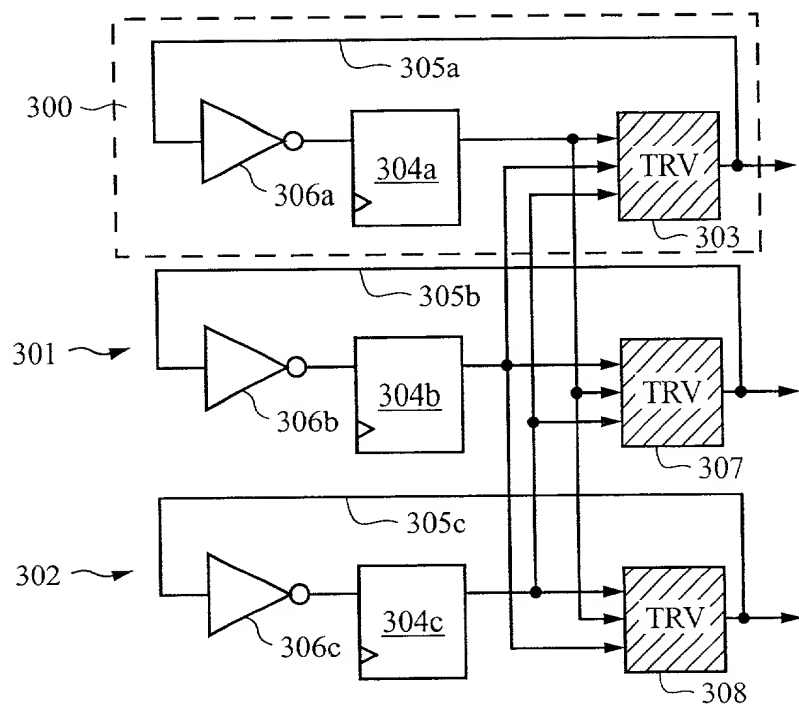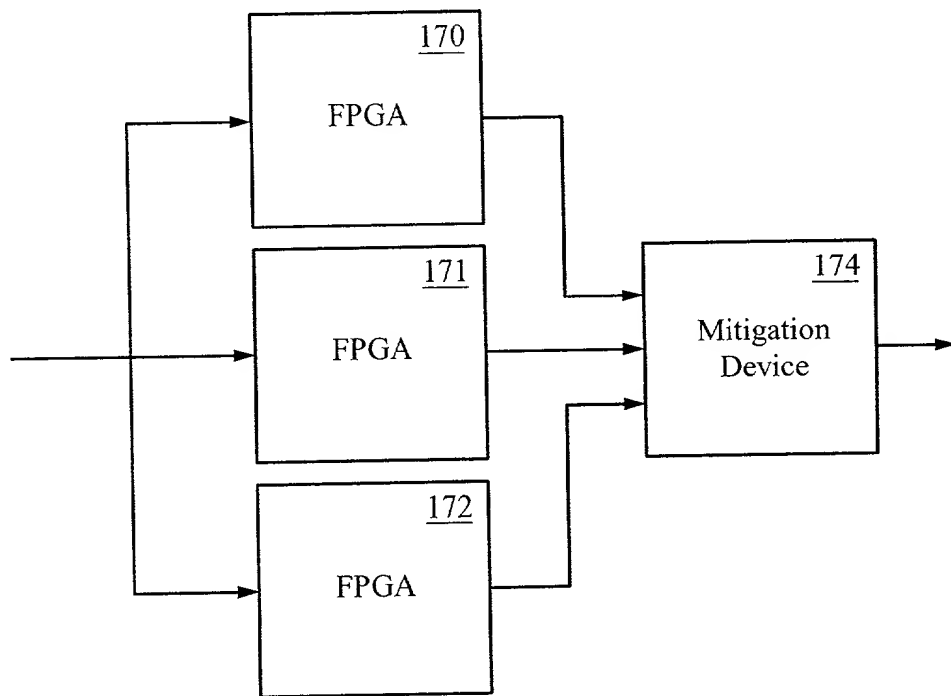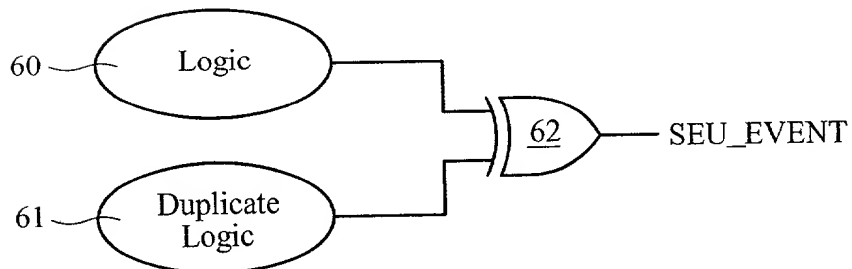
FIG. 8

FIG. 9

FIG. 10

Triple device redundancy

FIG. 11

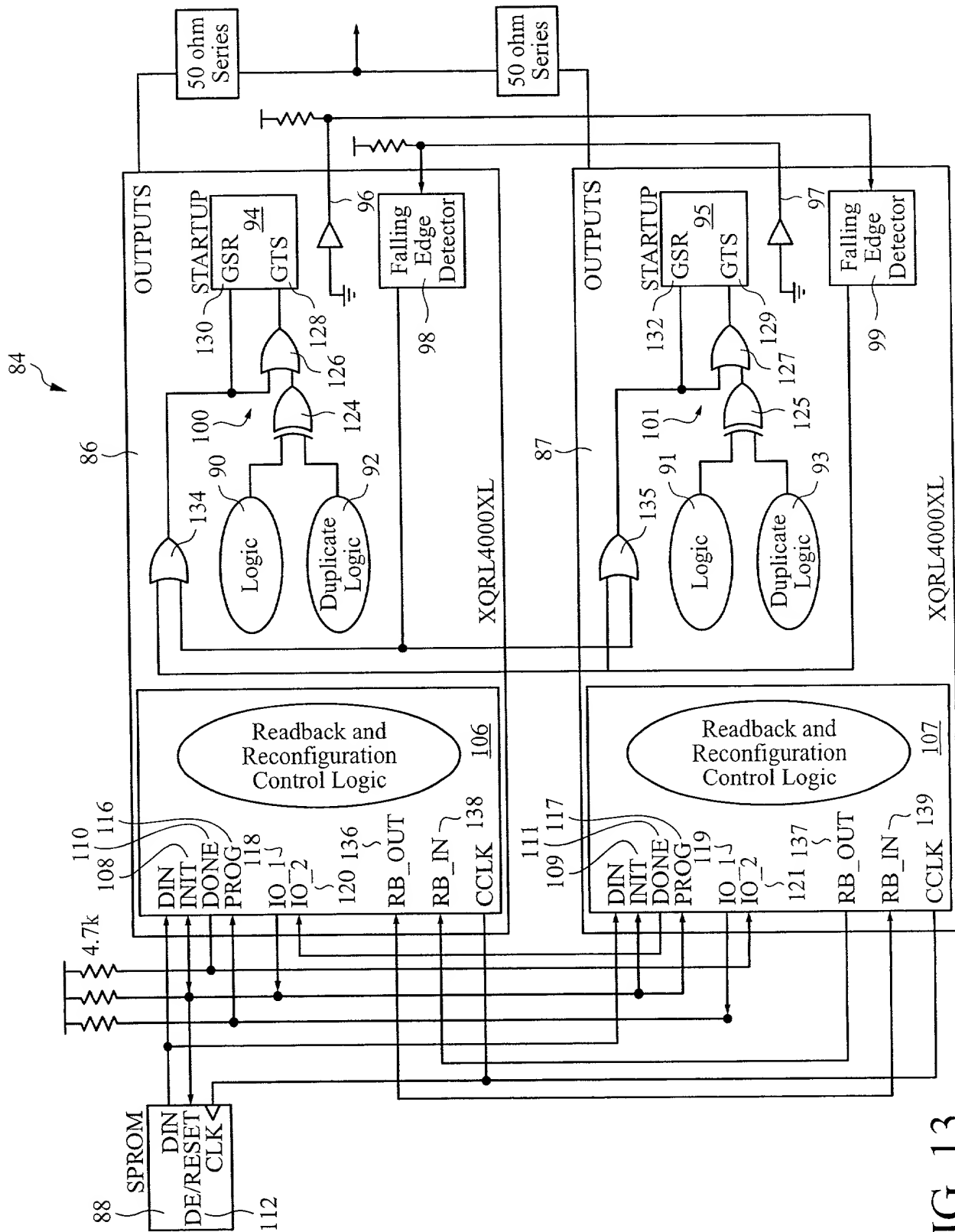SEU Detection by Reundancy and XOR Gating
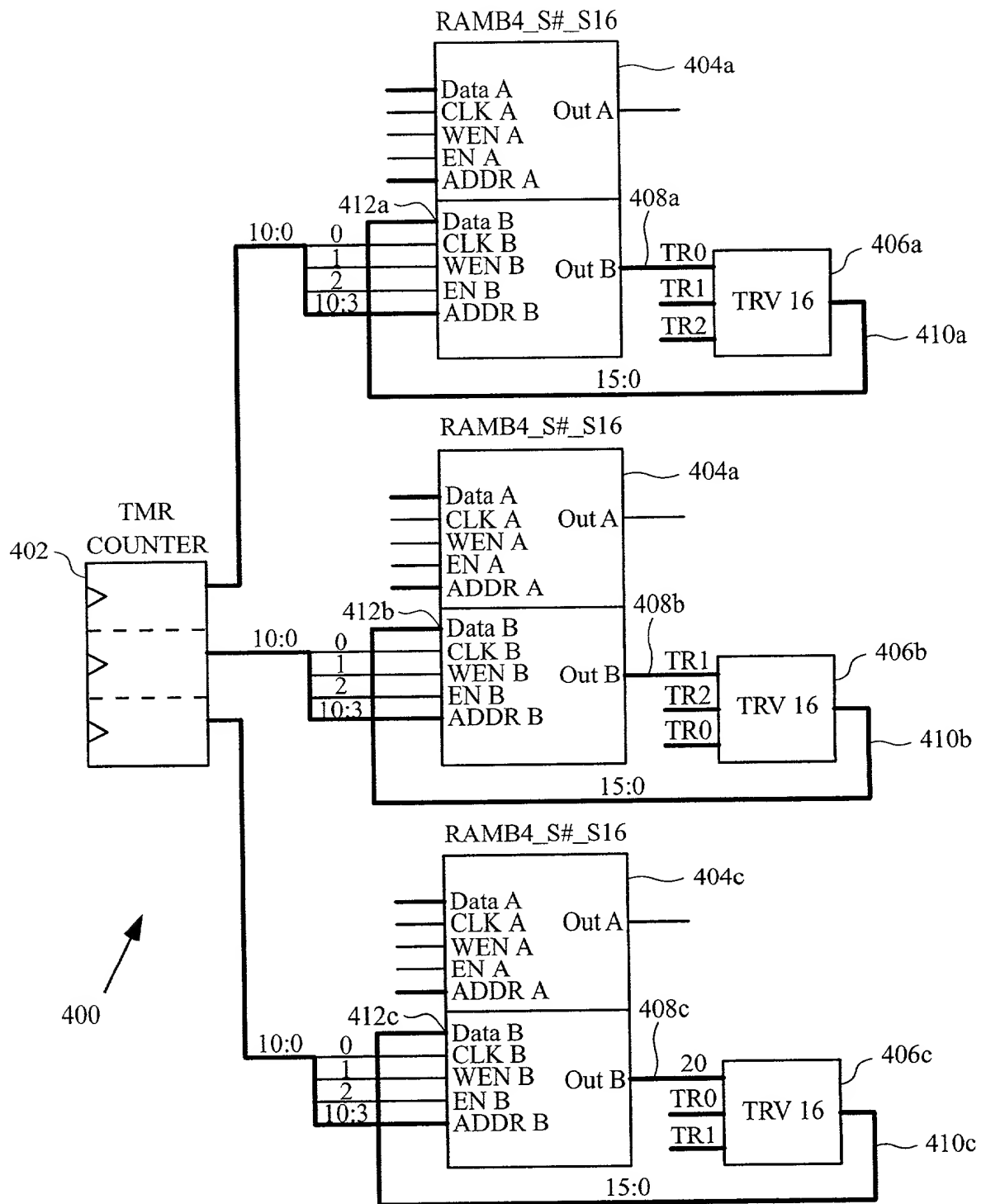
FIG. 12

FIG. 13

FIG. 14

FIG. 15

Memory

FPGA

DATA
ADDRESS
OE
CE

Configuration
Controller

SelectMAP
DATA(7:0)
WRITE
CS
BUSY
DONE
PROG
INIT
CCLK

Configuration Controller

182 — Memory
Interface

SelectMAP
Interface — 180

FSM

185 — CRC
Comparator

CRC
Calculator — 184

186

FIG. 16

Readback CRCComparator

FIG. 17

Redundant CRC Comparator
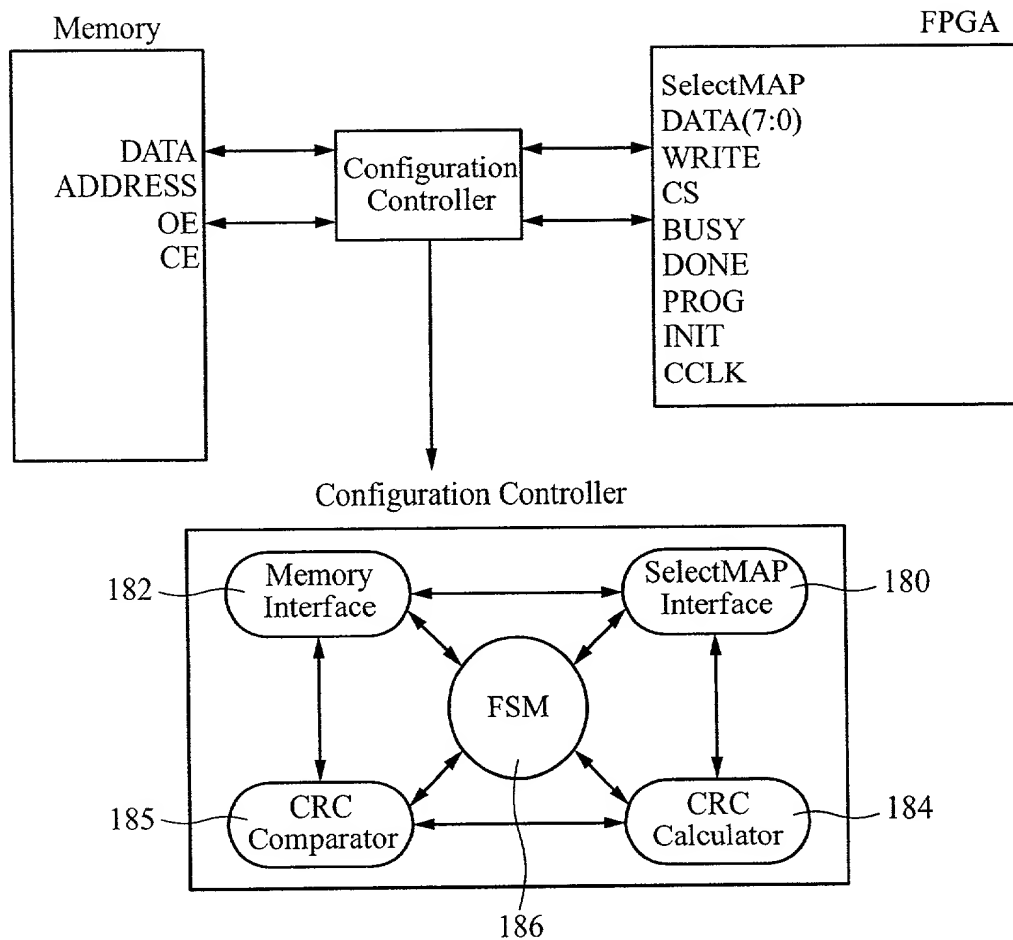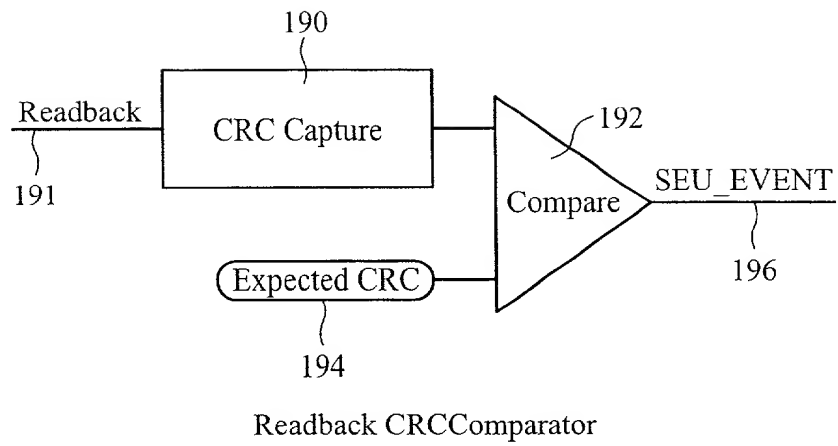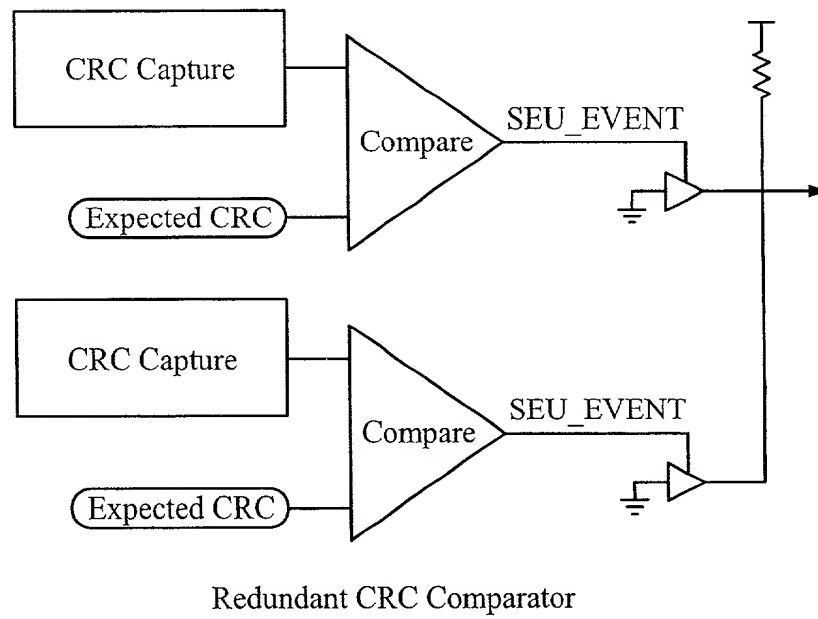
FIG. 18
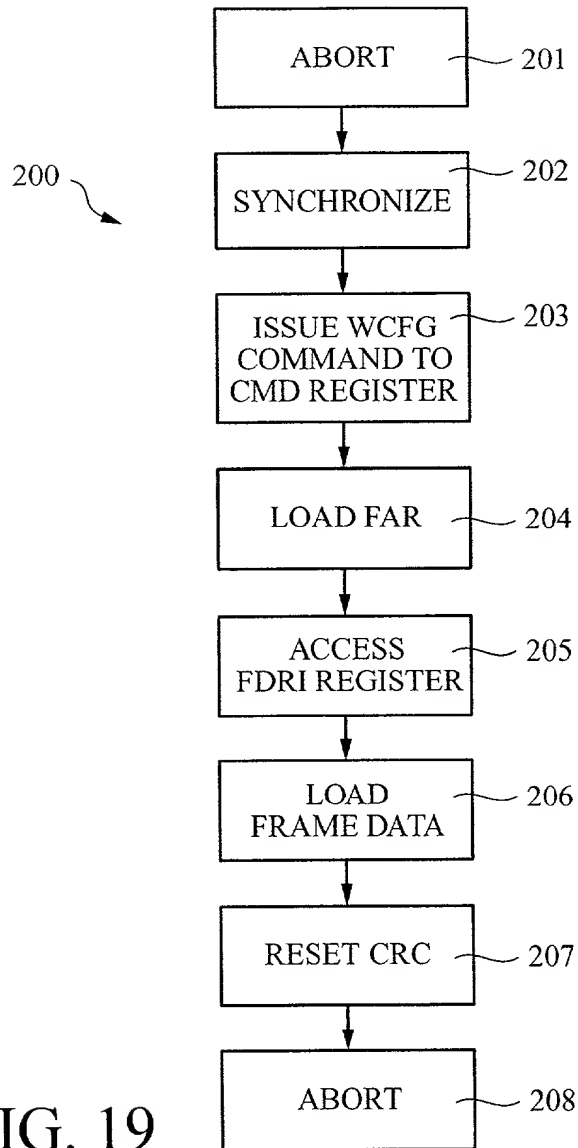
FIG. 19

Instruction Set for Single Frame Write Operation

Command		Data (32 Bits)
Synchronize		AA 99 55 66
Write to CMD		30 00 80 01
WCFG		00 00 00 01
Write FAR		30 00 20 01
Frame Address		0? ?? ?? 00
Write FDRI	XQVR300	30 00 40 2A
	XQVR600	30 00 40 3C
	XQVR1000	30 00 40 4E
Frame Data		
Write CMD		30 00 80 01
RCRC		00 00 00 07

FIG. 20

Scrubbing Control Circuit
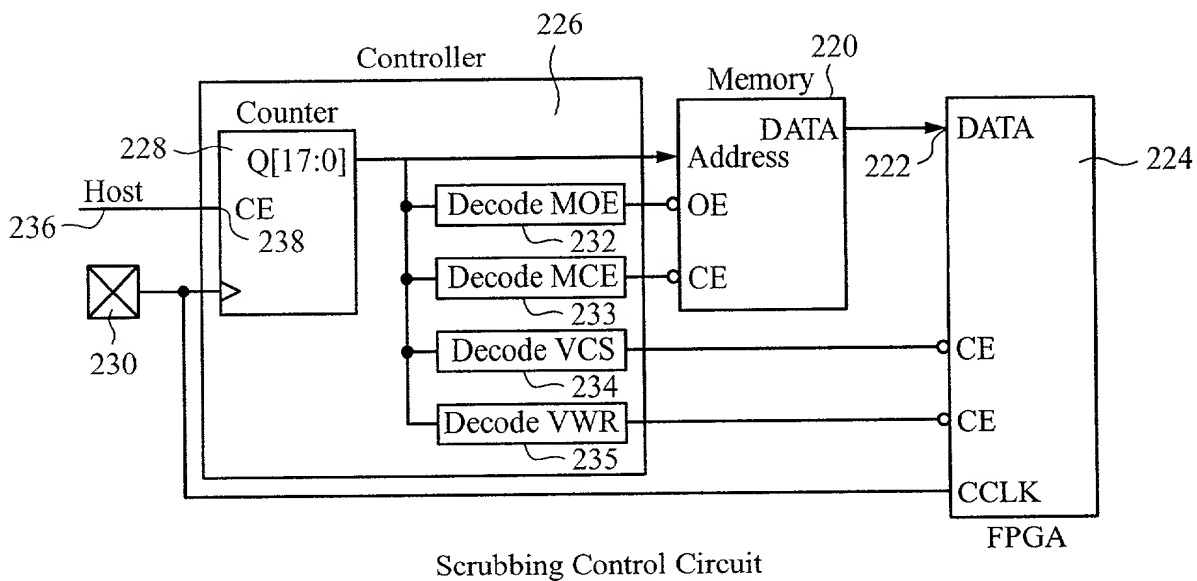
FIG. 21

Scrubbing State Transitions

States					Clock Cycles		
Type	MOE	MCE	VCS	VWR	XQVR300	XQVR600	XQVR1000
Load	L	L	L	L	207,972	435,312	745,596
Abort	H	H	L	H	4		
Disable	H	H	H	H	1		

FIG. 22